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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/757,405	01/08/2001	Guojin Liang	60012-0012	6397

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EXAMINER

CAO, CHUN

ART UNIT	PAPER NUMBER
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2115

DATE MAILED: 06/03/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/757,405

Applicant(s)

LIANG, GUOJIN

Examiner

Chun Cao

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 11 March 2004.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-30 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 5, 7 and 22-24 is/are allowed.
- 6) ☒ Claim(s) 1-4, 6, 8-21 and 25-30 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 11 March 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- ☒ Notice of References Cited (PTO-892)
- ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____
- ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- ☐ Notice of Informal Patent Application (PTO-152)
- ☐ Other: _____

FINAL REJECTION

1. Claims 1-30 are presented for examination. Claim 30 is a newly added claim.
2. The text of those applicable section of Title 35, U.S. Code not included in this action can be found in the prior Office Action.

Drawings

3. The drawings were received on 3/11/04. These drawings are accepted.
4. The rejections are respectfully maintained and reproduced infra for applicant's convenience.
5. Claims 1 and 30 are rejected under 35 U.S.C. 102(e) as being anticipated by Harrison (Harrison), US patent no. 6,173,432.

As per claim 1, Harrison discloses a multi-link receiving mechanism [fig. 5; col. 9, lines 31-36; emphasis added, col. 9, lines 34-35, "memory device 16" should be -- memory device 10-- typographical error], comprising:

a first receiver [memory device 10a, fig. 5] coupled to receive a first data stream and a clock signal [fig. 1; col. 1, line 61-col. 2, line 6; col. 4, lines 60-67], said first data stream comprising a first plurality of data units [col. 5, lines 37-41], said first receiver delaying said clock signal by a first variable delay to derive a first reference signal, and generating a first plurality of latching control signals based upon said first reference signal to latch said first plurality of data units [figures 2 and 3; col. 5, lines 2-6, 20-26, 37-41; col. 5, line 51-col. 6, line 12]; and

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a second receiver [memory devices 10b,10c, fig. 5; col. 9, lines 15-36] coupled to receive a second data stream and clock signal [fig. 1; col. 1, line 61-col. 2, line 6; col. 4, lines 60-67], said second data stream comprising a second plurality of data units [col. 5, lines 37-41], said second receiver delaying said clock signal by a second variable delay to derive a second reference signal, and generating a second plurality of latching control signals based upon said second reference signal to latch said second plurality of data units [figures 2 and 3; col. 5, lines 2-6, 20-26, 37-41; col. 5, line 51-col. 6, line 12].

As per claim 30 is written in means plus function format and contain the same limitations as claim 1, therefore, the same rejection is applied.

6. Claims 2-4, 6, 8-21 and 25-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Harrison (Harrison), US patent no. 6,173,432 in view of Applicant Admitted Prior Art (AAPA).

Harrison does not explicit teach the limitations as set forth in claims 2-3.

As per claim 2, AAPA teaches that first data stream and second data stream are not aligned with each other when received by said first receiver and said second receiver, respectively [page 3, lines 2-9].

As per claim 3, AAPA teaches that clock signal is not necessarily aligned with said first data stream or said second data stream [page 3, lines 19-21; page 4, lines 10-11].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Harrison and AAPA because they both teach of concurrently processing multiple data stream, and the specific teachings of

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AAPA stated above would maximize the functionality of Harrison system by allowing adjust the clock signal.

As per claim 4, AAPA discloses that first receiver adjust said first variable delay based upon relative alignment between said first data stream and said clock signal [page 5, lines 1-9].

As per claim 6, Harrison teaches that first variable delay and second variable delay are different delays [col. 6, lines 8-15].

As per claim 8, Harrison discloses that each of first plurality of data units occupies one data period, and wherein said first reference signal coincides approximately with a midpoint of a data period corresponding to one of first plurality of data units [col. 5, lines 19-25, 37-40]. AAPA also discloses the limitations as set forth in claim 8 [page 5, lines 1-5].

As per claim 9, Harrison discloses that each of second plurality of data units occupies one data period, and wherein said second reference signal coincides approximately with a midpoint of a data period corresponding to one of second plurality of data units [col. 5, lines 19-25, 37-40].

As per claim 10, Harrison discloses that each of first plurality of data units occupies one data period occupies one data period, and wherein said first receiver generates no more than one of said first plurality of latching control signals per data period [col. 8, lines 38-40].

As per claim 11, Harrison discloses that each of first plurality of latching control signals coincides approximately with a midpoint of a data period corresponding to one of first plurality of data units [col. 5, lines 19-25, 37-40].

As per claim 12, Harrison discloses that each of second plurality of data units occupies one data period occupies one data period, and wherein said second receiver generates no more than one of said second plurality of latching control signals per data period [col. 8, lines 38-40].

As per claim 13, Harrison discloses that each of second plurality of latching control signals coincides approximately with a midpoint of a data period corresponding to one of second plurality of data units [fig. 3; col. 5, lines 19-25, 37-40].

As per claim 14, Harrison discloses that first receiver comprises a first delay control mechanism for adjusting said first variable delay, and wherein second receiver comprises a second delay control mechanism for adjusting second variable delay [figs. 3 and 5; col. 6, lines 8-15; col. 9, lines 32-36].

As to claims 15 and 17, Harrison discloses that first delay control mechanism adjusts said first variable delay to cause said first receiver to generate said first plurality of latching control signals such that each of said first plurality of latching control signals coincides more closely with a midpoint of a data period corresponding to one of first plurality of data units [fig. 3; col. 5, lines 19-25, 37-40].

As to claims 16 and 18, Harrison discloses that second delay control mechanism adjusts said second variable delay to cause said second receiver to generate said first plurality of latching control signals such that each of said second plurality of latching

control signals coincides more closely with a midpoint of a data period corresponding to one of second plurality of data units [fig. 3; col. 5, lines 19-25, 37-40].

As to claims 19 and 20, Harrison discloses that first control delay mechanism comprises a detection mechanism such as a phase detector [fig. 3; col. 6, lines 66-67].

As per claim 21, Harrison discloses that first control mechanism further comprises a fixed delay element coupled to receive at least one of said first plurality of latching control signals and providing a delayed latching signal; and a latching component coupled to receive said first data stream, said latching component latching one of said first plurality of data units in response to said delayed latching signal [fig. 3; col. 5, lines 37-57].

As per claim 25, Harrison discloses that first receiver [memory devices 10a-c, fig. 5] comprises a first delay locked loop [fig. 3; col. 6, lines 13-29; col. 9, lines 32-36], and wherein second receiver [memory devices 10a-c, fig. 5] comprises a second delay locked loop [fig. 3; col. 6, lines 13-29; col. 9, lines 32-36].

As to claims 26 and 27, Harrison discloses that first delay locked loop generates no more than one of said first plurality of latching control signals per data period, and wherein each of said first plurality of latching control signals coincides approximately with a midpoint of a data period corresponding to one of first plurality of data units [fig. 3; col. 5, lines 19-25, 37-40].

As to claims 28 and 29, Harrison discloses that second delay locked loop generates no more than one of said second plurality of latching control signals per data period, and wherein each of said second plurality of latching control signals coincides

approximately with a midpoint of a data period corresponding to one of second plurality of data units [fig. 3; col. 5, lines 19-25, 37-40].

Allowable Subject Matter

7. Claims 5, 7 and 22-24 are allowed over prior art.
8. Applicant's arguments filed 3/11/2004 have been fully considered but are not persuasive.
9. In the remarks, applicants argued in substance that Harrison fails to 1) distinct first and second data streams as recited in the claim. 2) Harrison fails to distinct, separate, second reference signal from which are generated a second plurality of latching control signals as recited.
10. As to these points, 1) Harrison discloses a first receiver [memory device 10a, fig. 5] coupled to receive a first data stream [signals CA0-9] and a clock signal [fig. 1; col. 1, line 61-col. 2, line 6; col. 4, lines 60-67], and a second receiver [memory devices 10b, 10c, fig. 5; col. 9, lines 15-36] coupled to receive a second data stream [signals CA0-9] and clock signal [fig. 1; col. 1, line 61-col. 2, line 6; col. 4, lines 60-67]. In summary, the first and second data streams are distinct from each other. 2) Harrison teaches the claim limitation [see rejection on claim 1 above]; furthermore, Harrison discloses a second receiver [10b, or 10c, fig. 5] which delays clock signal by a second variable delay to derive a second reference signal [fig. 3; col. 5, lines 37-41; col. 5, line 51-col. 6, line 12; col. 8, lines 57-60].

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11. **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

Hand-delivered responses should be brought to Crystal Park II, 2121

Crystal Drive, Arlington, VA., Sixth Floor (Receptionist).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chun Cao at (703) 308-6106. The examiner can normally be reached on Monday-Friday from 7:30 am - 4:00 pm. If attempts to reach the examiner by phone are unsuccessful, the examiner's supervisor Thomas Lee can be reached at (703) 305-9717. The fax number for this Art Unit is following: Official (703) 872-9306.

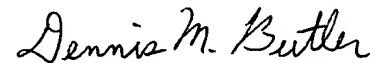
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Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 306-5631.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chun Cao

May 18, 2004



Dennis M. Butler
Primary Examiner